

**Amendments to the Specification**

Amend paragraph [0085] as follows:

--[0085] A voltage  $V_{pp}$  (for example, 12 V) inputted from an external ~~terminal~~ power source 26 is applied to a regulator circuit 27 via a resistance element 28. At this time, a voltage drop is caused by the resistance element 28 and a voltage  $V_{rpin}$  is inputted to the regulator circuit 27. A voltage  $V_{pll}$  (for example, 5 V) that is made constant and stabilized is inputted to the source side of the P-MOS transistor P1 and the P-MOS transistor P2.--

Amend paragraph [0086] as follows:

--[0086] The resistance value of the resistance element 28 inserted between the external ~~terminal~~ power source 26 and the input terminal of the regulator circuit 27 is set as follows. As described above, an erase current including the BTBT current, which is a leakage current of the flash memory, changes with time. The maximum value (initial state in the first erase pulse application) is set at 2 mA. In this case, to obtain a voltage  $V_{pll}$  of 5 V stabilized by the regulator circuit 27 even though the erase current has the maximum value, the resistance value  $R$  of the resistance element 28 can be  $\{12\text{ V} - 5\text{ V}\} / 2\text{ mA} = 3500\ \Omega$ . Consequently, the erase current is reduced with time and the voltage drop by the resistance element 28 is reduced. As a result, even when the input voltage  $V_{rpin}$  to the regulator circuit 27 is increased, the voltage  $V_{pll}$  of 5 V is output by the regulator circuit 27 in a stable manner. Therefore, the voltage  $V_{pll}$  can be constantly maintained at 5 V in a stable manner.--

Amend paragraph [0090] as follows:

--[0090] Subsequently, the first erase pulse application is performed as follows. First, a voltage  $V_{pp}$  (= 12 V) is inputted from the external ~~terminal~~ power source 26 to output a voltage  $V_{pll}$  of 5 V from the regulator circuit 27. At this time, since the threshold voltage of the memory cell is high immediately after the erase pulse application as described above, there is a large BTBT current as a leakage current and thus there is a large erase current including the BTBT current. Therefore, the voltage drop caused by the resistance element 28 is large. When the resistance value is set at  $3500\ \Omega$ , the input voltage  $V_{rpin}$  to the regulator circuit 27 is started at about 5 V.--

Amend paragraph [0099] as follows:

--[0099] As described above, in this embodiment, the voltage value of the erase pulse applied to the common source line 21 is set at a voltage  $V_{pll}$  stabilized to 5 V by supplying a voltage  $V_{rpin}$  to the regulator circuit 27, the voltage  $V_{rpin}$  being obtained by dropping a voltage  $V_{pp}$  (12 V) of the external ~~terminal~~ power source 26 with the resistance element 28 of 3500  $\Omega$ . Then, the level detection circuit 22 judges the termination of the first erase pulse application based on a comparison result between the reference voltage  $V_{ref}$  of 11 V and the input voltage  $V_{rpin}$  to the regulator circuit 27 which has a voltage magnitude of about 6 V or larger after starting at 5 V at the start of the erase operation.--

Amend paragraph [0103] as follows:

--[0103] In the first embodiment, the voltage applied to the common source line 21 is the voltage  $V_{pp}$  (for example, 12 V) inputted from the external ~~terminal~~ power source 26. In general, however, a nonvolatile semiconductor memory such as a flash memory has a single power source. Various voltages required for respective modes as shown in Table 1 are generated by an internal charge pump circuit for boosting a voltage.--

Amend paragraph [0104] as follows:

--[0104] In this embodiment, a voltage  $HV_{pp}$  boosted by a voltage boosting circuit (voltage boosting charge pump circuit in the nonvolatile semiconductor memory) 41 is used instead of the voltage  $V_{pp}$  from the external ~~terminal~~ power source 26 used in the first embodiment. Thus, a more practical configuration of a nonvolatile semiconductor memory is achieved. Here, the voltage  $HV_{pp}$  is about 10 V.--

Amend paragraph [0108] as follows:

--[0108] As a result, the same effect as in the first embodiment can be obtained. In this embodiment, since the voltage  $HV_{pp}$  is internally generated by the voltage boosting circuit 41, the external ~~terminal~~ power source 26 for capturing the voltage  $V_{pp}$  is not required unlike the first embodiment.--

Amend paragraph [0110] as follows:

--[0110] Furthermore, in the above embodiments, the termination of the first erase pulse application is judged based on an increase attributable to the decrease of the erase current

value of the voltage value supplied from the external ~~terminal~~ power source 26 or the voltage boosting circuit 41 to the regulator circuit 27, 39 via the resistance element 28, 40. However, this invention is not limited to this method. The decrease of the erase current value shown in Fig. 13 may be directly detected and the termination of the first erase pulse application may be judged based on this detection result.--